Design and Optimization of a Low-Power, High-Speed Hybrid 10T Full Adder

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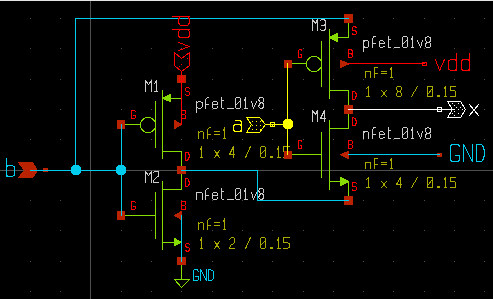
# **Abstract**—This paper presents the design and optimization of a Hybrid 10T full adder in SkyWater 130nm CMOS technology, targeting high speed and low power consumption. The Hybrid 10T architecture reduces propagation delay compared to traditional designs.Design aims power consumption below 100 µW and a propagation delay of approximately 300 ps, demonstrating significant performance improvements.

# **Keywords**—Hybrid 10T adder, low power, high speed, SkyWater 130nm, CMOS technology.

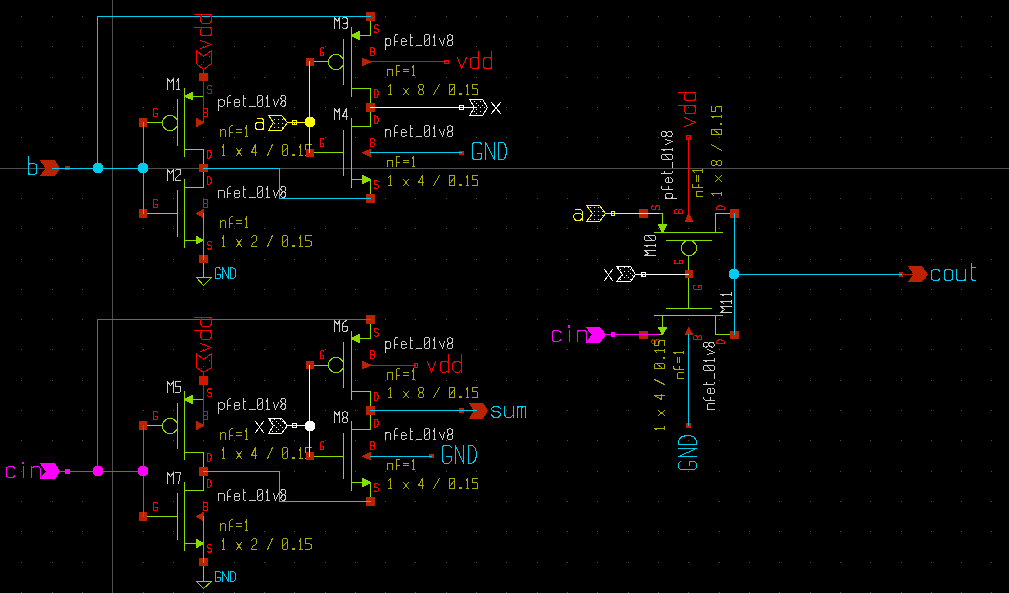
# **Introduction**

The increasing demand for high-performance, energy-efficient integrated circuits in digital computing, especially in artificial intelligence applications, highlights the critical role of full adders in arithmetic logic units. Traditional full adder designs often struggle to balance speed and power consumption, leading to higher energy usage and delays. This paper discusses the design and optimization of a Hybrid 10T full adder in SkyWater 130nm technology, achieving significant gains in power and speed over conventional designs.

**Design Overview**

1. Hybrid 10T Full Adder: :- Architecture: Combines the strengths of pass-transistor and CMOS logic with 10 transistors, effectively reducing propagation delay while enhancing power efficiency. The 10T design maintains signal integrity better than lower transistor count designs, like 6T and 8T, while achieving a balance between speed, power, and reliability. 

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| Figure 1 . 4T XOR gate Schematic |

Figure 2. Hybrid 10 T Full Adder circuit schematic

**Improvements**

During the design of the Hybrid 10T full adder, challenges included balancing power consumption with speed and ensuring adequate noise margins for signal integrity. To address these issues, future improvements could focus on optimizing transistor sizing and circuit layout to reduce parasitic effects. Additionally, exploring alternative architectures or technologies may enhance performance further.

**Conclusion**

This paper presented the design of a Hybrid 10T full adder implemented in Sky Water 130nm CMOS technology, achieving significant improvements in power consumption and speed, respectively. The Hybrid 10T architecture outperforms traditional 6T and 9T designs, making it well-suited for modern applications in artificial intelligence and high-performance computing. Future work will focus on further optimizing the design and exploring its integration into larger digital systems.

**References**

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